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HOGAN & HARTSON LLP
IP GROUP, COLUMBIA SQUARE
555 THIRTEENTH STREET, N.W.
WASHINGTON, DC 20004

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/689,716
Filing Date: October 22, 2003
Appellant(s): GONZALEZ ET AL.

Kevin G. Shaw

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 20, 2007 appealing from the Office action mailed July 14, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-7, 29, 30, 32-34, 41, 44-48, and 50-52.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20040088469A1	LEVY	5-2004
6,295,566	STUFFLEBEAM	9-2001
5,546,530	GRIMAUD	8-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code 103(a) not included in this action can be found in a prior Office action.

1. Claims 1-7, 29, 30, 32-34, 41, 44-48 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) in view of Stufflebeam (US006295566B1), further in view of Grimaud (US005546530A).

2. As per Claim 1, Levy teaches chipset (104) for managing data transfers within computing device [0014]; scalable interconnect (Device 0) connecting to computing device [0021]; and plurality of ports or high-speed video card slots [0016] connected to interconnect [0021], high speed video card slots including at least one 1st video card slot and 2nd video card slot [0016]. According to Applicant's disclosure, a "high speed video card slot" is defined as PCI Express video card slot [00057]. Levy teaches one or more devices (DEVICES 1-5) comprise video cards [0016]. Device interfaces of DEVICES 0-5 have ports that provide a physical interface for establishing lanes between the devices. A link comprises lanes which are grouped together to form a communications path between the devices [0018]. These links are PCI Express links

[0001]. So, Levy teaches video cards are connected to system through PCI Express links, and so Levy is considered to teach PCI Express video card slots, which are high speed video card slots.

However, Levy does not teach computing device is a motherboard and motherboard enables first and second card to attach, respectively, to at least one first card slot and second card slot, and wherein motherboard enables first and second card to operate concurrently to output data. However, Stufflebeam teaches interconnect connecting to motherboard (c. 4, ll. 48-50; c. 4, ll. 59-61); and plurality of high-speed card slots connected to interconnect (c. 6, ll. 23-35). When user wishes to attach additional card, power is removed from card slot that card is to be attached to. After inserting card into slot, the software identifies and configures the additional card in the slot so that the first and second card can operate in parallel to output data (c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; c. 1, ll. 21-25), and the cards can include video cards (c. 5, ll. 7-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Levy so computing device is a motherboard as suggested by Stufflebeam. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new features to the machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. The motherboard, by enabling pluggable components, allows users to personalize a computer system depending on their applications and needs. It would have been obvious to modify the device so motherboard enables first and second card to attach, respectively, to the at least one first card slot and second card slot, and wherein the motherboard enables the first and the second card to operate concurrently to output data as suggested by Stufflebeam because Stufflebeam suggests faster processing (c. 1, ll. 21-25).

However, Levy and Stufflebeam do not expressly teach both cards are video cards, and video cards output graphics data to a single visual display device. However, Grimaud teaches attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (c. 2, ll. 40-44, c. 2, ll. 53-65; c. 7, ll. 39-40).

It would have been obvious to modify devices of Levy and Stufflebeam so display area of display is divided into first and second sections, first video card performing graphics processing related to first section; and second video card performing graphics processing related to second section as suggested by Grimaud because Grimaud suggests this ensures single graphics element is not overburdened with its rendering task by allowing dynamic adjustment of each graphics element so graphics elements take approximately the same time to render their respective images, and video cards can operate on these divided sections in parallel, therefore allowing different graphics machines to be connected together to render complex images faster than any one of them taken separately would be able to render (c. 5, ll. 55-c. 6, ll. 12; c. 7, ll. 10-40).

3. As per Claim 2, Levy teaches switch (116) connected to interconnect (Device 0), switch distributes bandwidth from interconnect to high-speed video card slots [0021, 0017, 0018, 0016].

4. As per Claim 3, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection, and wherein the switch (116, Fig. 3) distributes bandwidth from the x16 connection to two x16 video card slots [0001, 0021, 0017, 0018, 0016].

5. As per Claim 4, Levy teaches interconnect comprises at least a x32 connection [0001].

6. As per Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Fig. 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

7. As per Claim 6, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001. 0016].

8. As per Claim 7, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect having a connection having at least 24 lanes, and wherein interconnect is divided into x8 connection between chipset (104, Fig. 1) and one of plurality of high-speed video card slots and x16 connection between chipset and another of plurality of high-speed video card slots [0001, 0016].

9. As per Claim 29, Levy teaches interconnect supports links between chips that have x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect have 1st x16 connection to 1st video card slot and 2nd smaller-scaled connection to 2nd video card slot [0001, 0016].

10. As per Claims 30 and 46, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at

least x1 links, leaving chips to optionally support the other link widths. Levy gives an example wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

11. As per Claims 32 and 47, Levy teaches ports or peripheral slot connected to interconnect (Device 0, Fig. 2). In Fig. 2, peripheral slot is shown to have prespecified dimensions a x8 link, and first dimensions are for x4 link and x8 link [0020]. So, Levy teaches peripheral slot having second prespecified dimensions, wherein second dimensions differs from the first dimensions.

12. As per Claim 33, Levy describes that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy discloses first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots.

13. As per Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

14. A per Claim 41, Levy teaches computing device for supporting multiple video cards, computing device having processor socket 104 adapted to receive processor 102 [0014]; single scalable interconnect (Device 0) provides data paths to processor socket (Fig. 1), scalable interconnect is selectively divided as needed to allocate data paths [0016-0017]; and plurality of high-speed video card slots connected to interconnect, each video card slot has first prespecified dimensions and is specifically adapted for coupling to video card [0001, 0021, 0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and the motherboard is capable of receiving and facilitating

concurrent operation of a first and a second card to output data. However, Stufflebeam describes that the computing device is a motherboard (c. 4, ll. 48-50), the processor is a central processing unit (CPU) (100, Fig. 1; c. 4, ll. 40-46), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data (c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; c. 1, ll. 21-25), wherein the cards can include video cards (c. 5, ll. 7-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so the processor is a CPU as suggested by Stufflebeam. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. It would have been obvious to modify the device so that the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data for the same reasons given in the rejection for Claim 1.

However, Levy and Stufflebeam do not teach that the cards are substantially similar video cards and operate to output graphics data to a single visual display device. However, Grimaud teaches this limitation, as discussed in the rejection for Claim 1.

15. As per Claim 44, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths, so, Levy teaches each of video card slots is configured to couple with graphics card designed to be used with x16 connection [0001, 0016].

16. As per Claim 45, Levy teaches that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. So, Levy teaches an interconnect

(Device 0, Fig. 1) comprising a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

17. As per Claim 48, Levy teaches a high performance computer including a scalable interconnect (Device 0) including a first and a second provides data paths, wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017], and a first and a second video slots, wherein the first and the second video slots connect, respectively, to the first and second data paths [0020], the first data path being equal to or larger in scale than the second data path, wherein the first and the second video slots have a substantially similar physical configuration [0001], as discussed in the rejection for Claim 42, and wherein the video slot physical configuration is selected to allow the first and the second video slots to accept a graphics card; and a first graphics card coupled to the first video slot [0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and a second graphics card coupled to the second video slot, wherein first and second video cards operate concurrently to output graphics data to a display device. However, Stufflebeam teaches that the computing device is a motherboard (c. 4, ll. 48-50), the processor is a CPU (100, Fig. 1; c. 4, ll. 40-46), and a second card coupled to the second slot, wherein first and second cards operate concurrently to output data (c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; c. 1, ll. 21-25), wherein the cards can include video cards (c. 5, ll. 7-19). This would be obvious for the same reasons given in the rejection for Claim 41.

18. As per Claims 50-52, Levy does not teach a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the

first section; and the second video card performing graphics processing related to the second section. However, Grimaud teaches a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section (c. 2, ll. 40-44, 53-65). This would be obvious for the same reasons given in the rejection for Claim 1.

(10) Response to Argument

1. Applicant's arguments filed August 16, 2007 are fully considered but are not persuasive.

2. Applicant argues Levy (US 20040088469A1) merely states attached devices may include "video cards." Levy fails to suggest "a plurality of high speed video card slots...including at least one first video card slot and second video card slot." Levy does not provide disclosure regarding attachment and operation of 2 or more high speed video cards. Levy does not provide disclosure regarding slots for receiving multiple high speed video cards. Levy only suggests examples of components useable on a motherboard but does not suggest the features of Claim 1. Levy does not provide any disclosure that would enable the features of Claim 1 (p. 11).

In reply, the Examiner points out that according to Applicant's disclosure, a "high speed video card slot" is defined as a PCI Express video card slot [00057]. Levy teaches that one or more devices (DEVICES 1-5) comprise video cards [0016]. The device interfaces of the DEVICES 0-5 comprise ports that provide a physical interface for establishing lanes between the devices. A link comprises lanes which are grouped together to form a communications path between the devices [0018]. These links are PCI Express links [0001]. Therefore, Levy teaches that video cards are connected to the system through PCI Express links, and therefore Levy is considered to teach PCI Express video card slots, which are high speed video card slots. Even

though Levy does not explicitly teach that more than one video card is attached to their respective video card slots at a time and than the video cards operate in parallel, Grimaud (US005546530A) was used to teach attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (c. 2, ll. 40-44, c. 2, ll. 53-65; c. 7, ll. 39-40). Therefore, the device of Levy can be modified so that more than one video card is attached to their respective high speed video card slots at a time and than the video cards operate in parallel, as suggested by Grimaud. Therefore, the combination of Levy and Grimaud is considered to teach a plurality of high speed video card slots as recited in Claim 1.

3. Applicant argues that there is no suggestion in Stufflebeam (US006295566B1) that the invention is further related to enhancement of motherboard design to include previously unfound features of multiple video card slots. Stufflebeam merely provides that video cards can be added to a motherboard without providing that multiple video cards can be concurrently connected to a motherboard, and that the motherboard provides multiple high-speed video card slots (p. 12).

In reply, the Examiner points out Levy was used to teach multiple high-speed video card slots, as discussed above. Stufflebeam was used to teach multiple cards can be concurrently connected to a motherboard (c. 1, ll. 21-25; c. 3, ll. 31-33; c. 3, ll. 56-c. 4, ll. 17; c. 4, ll. 48-50, 59-61; c. 5, ll. 7-19; c. 6, ll. 23-35). So, device of Levy can be modified so multiple cards can be concurrently connected to a motherboard through the multiple high-speed video card slots, as suggested by Stufflebeam. Grimaud was used to teach attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (c.

2, ll. 40-44, c. 2, ll. 53-65; c. 7, ll. 39-40). So, the Levy-Stufflebeam combination can be modified so that multiple video cards can be concurrently connected to a motherboard through the multiple high-speed video card slots, as suggested by Grimaud. So, the combination of Levy, Stufflebeam, and Grimaud is considered to teach the limitations as they are recited in the claims.

4. Applicant argues that the previous Office Action also failed to adequately consider Applicants' Declaration Under 37 CFR 1.132. In response, the Action cites to Grimaud in support of the proposition that multiple graphic processors systems are quite known. This response fails to address Appellant's evidence that motherboards having multiple high-speed graphics slots, particularly having a scalable bus system, did not exist prior to Appellant's conception and commercialization of the present invention as claimed. Even if the multiple graphics processors may be connected to a motherboard via expansion slots, this does not address the present invention's claimed multiple high-speed graphics slots (pages 12-13).

In reply, the Examiner points out Levy teaches having multiple high-speed graphics slots, as discussed above, and also teaches having scalable bus system ([0075], Abstract). Levy's application was filed on October 30, 2002, which is prior to Applicant's filing date of October 22, 2003. Since this has been known prior to Applicant's filing date and this is similar to what Applicant is claiming, record is considered to establish sufficiently strong case of obviousness that object evidence of nonobviousness is not sufficient to outweigh evidence of obviousness. In view of the foregoing, when all of the evidence is considered, totality of rebuttal evidence of nonobviousness fails to outweigh evidence of obviousness. So, declaration under 37 CFR 1.132 is still considered to be insufficient to overcome rejection as set forth in last Office action.

5. Applicant argues that the Grimaud specification contains a single passage regarding the addition of graphics processors through available slots. There is no further suggestion in Grimaud that the computer contains multiple high-speed video card slots. "Video card slot" has a well defined meaning in the computer industry (not merely a slot for accepting a video card), and none of the three cited references contain the feature of multiple video card slots (page 13).

In reply, Examiner disagrees that "video card slot" has a well defined meaning in the computer industry other than a slot for accepting a video card. One of ordinary skill in the art would define "video card slot" to be a slot for accepting a video card. Since the claims merely recite "video card slot", and do not further define what exactly "video card slot" is, "video card slot" is interpreted to be a slot for accepting a video card. The combination of Levy and Grimaud is considered to teach multiple high-speed video card slots, as discussed above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joni Hsu

Conferees:

Ulka Chauhan

Kee Tung

KEE M. TUNG
PATENT EXAMINER

KEE M. TUNG
SUPERVISORY PATENT EXAMINER

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER